CLAIMS

What is claim is:

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- 1. A thin-film transistor structure, at least essentially mainly 5 comprising:
 - an insulating substrate;
 - a gate electrode on said insulating substrate;
 - a dielectric layer over said gate electrode;
 - a first semiconductive layer on said dielectric layer;
 - a second semiconductive layer on said first semiconductive layer;
 - a first conductive layer on said second semiconductive layer;
 - a second conductive layer on said first conductive layer, said second conductive layer is used as a source and a drain;
 - a third conductive layer on said second conductive layer; and
 - an opening through said second semiconductive layer, said first conductive layer, said second conductive layer and said third conductive layer and exposing said first semiconductive layer.
- 2. The thin-film transistor structure according to claim 1, wherein said gate electrode comprises an AlNd gate electrode.
 - 3. The thin-film transistor structure according to claim 1, wherein said dielectric layer comprises a silicon nitride layer.

- 4. The thin-film transistor structure according to claim 1, wherein said first semiconductive layer comprises a hydrogenated amorphous silicon layer.
- 5. The thin-film transistor structure according to claim 1, wherein said second semiconductive layer comprises an N-type amorphous silicon layer.
 - 6. The thin-film transistor structure according to claim 1, wherein said first conductive layer prevent said second conductive layer and said second semiconductive layer from diffusing into each other.
 - 7. The thin-film transistor structure according to claim 1, wherein said third conductive layer is used as a glue layer and protects said second conductive layer from being over-etched.
 - 8. The thin-film transistor structure according to claim 1, wherein said first conductive layer, said second conductive layer and said third conductive layer comprise a sandwich structure of AlNdN, AlNd and AlNdN alloys.
 - 9. A thin-film transistor structure, at least comprising:
 - an transparent insulating substrate;

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- a gate electrode on said transparent insulating substrate;
- a dielectric layer over said gate electrode;
- a first semiconductive layer on said dielectric layer;
 - a second semiconductive layer on said first semiconductive layer;

a first AlNdN alloy layer on said second semiconductive layer;

an AlNd alloy layer on said first AlNdN alloy layer, said AlNd alloy layer is used as a source and a drain;

a second AlNdN layer on said AlNd alloy layer; and

an opening through said second semiconductive layer, said first AlNdN alloy layer, said AlNd alloy layer and said second AlNdN layer and exposing said first semiconductive layer.

- 10. The thin-film transistor structure according to claim 9, wherein said first AlNdN alloy layer has a thickness of about 500 angstroms.
 - 11. The thin-film transistor structure according to claim 9, wherein said AlNd alloy layer has a thickness of about 2000 angstroms.
- 12. The thin-film transistor structure according to claim 9, wherein said second AlNdN alloy layer has a thickness of about 500 angstroms.
 - 13. A thin-film transistor structure, said thin-film transistor structure comprising:
- 20 an insulating substrate:
 - a gate electrode on said insulating substrate;
 - a dielectric layer over said gate electrode;
 - a hydrogenated amorphous silicon layer on said dielectric layer;
- an amorphous silicon layer on said hydrogenated amorphous silicon layer;

a first conductive layer on said amorphous silicon layer;

an AlNd alloy layer on said first conductive layer, said AlNd alloy layer is used as a source and a drain; and

- a second conductive layer on said AlNd alloy layer, said second conductive layer is used as a glue layer and to protects said AlNd alloy layer from being over-etched.
- 14. The thin-film transistor structure according to claim 13, wherein said first conductive layer prevents said AlNd alloy layer and said amorphous silicon layer from diffusing into each other.
- 15. The thin-film transistor structure according to claim 13, wherein said first conductive layer and said second conductive layer comprise AlNdN alloy layers.

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